AMENDMENTS TO THE DRAWINGS

The attached sheets of drawings includes changes to Figs. 1 and 4. In addition, the top margin has been corrected on all sheets. These sheets replace the formal drawing sheets.

Attachment: Replacement Sheet(s)

REMARKS

Reconsideration and allowance of the subject application are respectfully requested.

As a formal matter, Applicants have corrected the formal drawings in which transcription errors were made from the originally filed drawings. Specifically, the right-most block of Figure 1 of the promoted data word now labeled p3 is labeled p0. Moreover, arrows of Figure 4 were offset by one block and have been corrected. Approval of the replacement sheets 1 and 3 is respectfully requested. Margins for all sheets have also been corrected.

All claims 1-15 stand rejected under 35 U.S.C. §102(b) as being clearly anticipated by Julier et al., U.S. Patent 6,081,824. This rejection is respectfully traversed.

A single prior art reference only anticipates a claim if expressly or inherently describes each and every limitation set forth in the claim. *Verdegaal Bros., Inc. v. Union Oil Co., Inc.*, 814 F.2d 628, 631 (Fed. Cir. 1987). Julier fails to satisfy this rigorous standard.

The claims provide a new data processing instruction within a data processing system that may serve to unpack data values held within a data word and also perform a single-instruction-multiple-data type arithmetic operation on the unpacked data values. Unpacking non-adjacent data values within the data word may be implemented with considerably less overhead than conventional unpacking instructions that unpack adjacent data values. In particular, the need for additional data pathways that can diverge the bit positions of previously adjacent data values may be avoided. Instead, for example, already-present masking and word shifting circuitry may be utilized. Furthermore, the simplification of the unpacking functions enables a single instruction to be used to both unpack and perform arithmetic operations on the operands

derived from the first input data value and a second, different input data value without introducing processing cycle constraint problems.

Julier is directed to an entirely different problem related to dividing unsigned integers. Figures 3 and 4 represent a way of calculating the quotient $Y/2^{(N-1)}$. Julier does not disclose using a single instruction to generate a result value obtained by unpacking non-adjacent, multibit values corresponding to a first input data word and performing arithmetic operations using respective bit portions of a second, different input data word.

The Examiner contends that Figure 2B of Julier discloses promotion of a data word, and Figure 2A discloses performing independent arithmetic operations on a plurality of multibit portions of a first packed operand 230 and another packed operand 240. The Examiner also makes reference to Figures 3 and 4, and columns 41-52. Neither the packed "add" instruction illustrated in Figure 2 nor the packed "shift" instruction illustrated by Figure 2B disclose an operation that yields a result value given by:

(iv) selecting a plurality of non-adjacent multibit portions of said first input data word to form a plurality of multibit portions each of bit length A;

(iv) optionally shifting said plurality of non-adjacent multibit portions by a common shift amount to shifted bit positions;

(vi) promoting each of said plurality of non-adjacent multibit portions from said bit length of A to a bit length of B to form a plurality of promoted multibit portions, such that said promoted multibit portions may be abutted to form a promoted data word.

Column 4 of Julier describes the packed "add" instruction of Figure 2A and the packed "shift" instruction of Figure 2B as <u>independent</u> operations. Julier fails to disclose performing both instruction operation on input operands to yield a result data word.

Notwithstanding the Examiner's contention, Applicants do not find any teaching in Julier of "selecting a plurality of non-adjacent multibit portions of said first input data word to form a plurality of multibit portions each of bit length A." The Examiner refers to the result data word 280 in Figure 2B. But this is a result data word rather than an input data word from which result value is determined. Julier also does not *select* non-adjacent elements from either input operand 260 and 270. All of the data elements in the operands 260 and 270 are "selected," and those data elements are clearly adjacent. Furthermore, Julier does not disclose "promoting each of said plurality of non-adjacent multibit portions." Again, claim 1 specifies that the non-adjacent multibit portions which are promoted are from "said first input data words" rather than a result word such as that shown in 280 in Figure 2B.

Column 6, lines 41-54 of Julier, to which the Examiner makes reference in paragraph 2 of the office action, describes Figure 4. This passage disclose that a 16-bit input operand Y is right-shifted by 8 bits. The most significant 8 bits are filled by zeros, and the least significant 8 bits are filled by the values previously occupying the most significant 8 bits. Subsequently, a value X is added to the shifted value of Y. The value X that is added to the shifted value of Y at stage 460 of Figure 4 is obtained by copying the input operand Y, clipping the duplicated value, and adding a biasing value to the clipped duplicate value (at stage 440). Similarly, in Figure 3, the addition operation performed at stage 350 involves adding to the right-shifted value of the input operand Y a value obtained by copying the value of the input operand and then clipping and biasing that copied value.

Accordingly, Julier does not disclose the claimed feature where the instruction decoder is operable to perform an operation based on a first input data word and a second, different input data word to yield a result value given by the operations specified at claim integers (iv) to (vii) of

claim 1. Rather, in Figures 3 and 4, a single input operand is copied and manipulated to provide the second operand of the arithmetic operation represented by the addition of stages 350 and 460 of the flow charts of Julier.

Thus, the combination of features in claim 1 are neither disclosed nor suggested in claim 1. Independent method claim 14 cites similar features to that of claim 1, and therefore, is not anticipated by Julier for the reasons set forth above.

The application is now in condition for allowance. An early notice to that effect is earnestly solicited.

Respectfully submitted,

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